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EXAMINER	
LOKE, STEVEN HO YIN	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/421,217	Applicant(s) TAKAHASHI, HIDEKI	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-26 and 40-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-26, 40-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. Claims 22-26 and 40-44 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 3 discloses a first pair of channel regions [53] formed adjacent to a first gate electrode [49] on the right side of the device and a second pair of channel regions [53] formed adjacent to a second gate electrode [49] on the left side of the device. Therefore, there are at least four channel regions in the device. The specification never discloses a control electrode facing the portions through the insulating film so that the portions form channel regions as only channel regions of the insulated gate semiconductor device as claimed in claims 22 and 40.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 22, 24, 26, 40, 42 and 44 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kinzer.

In regards to claim 22, Kinzer shows all the elements of the claimed invention in fig. 19. It is an insulated gate semiconductor device, comprises: a first semiconductor layer [50] of a first conductivity type (p) having first and second main surfaces on opposite

sides thereof; a second semiconductor layer [52] of a second conductivity type (n) provided on the first main surface of the first semiconductor layer; a third semiconductor layer [61, 62] of the second conductivity type higher in an impurity concentration (n+) and thinner than the second semiconductor layer [52], and provided on a surface of the second semiconductor layer [52]; a fourth semiconductor layer [81] of the first conductivity type provided on a surface of the third semiconductor layer [61, 62], wherein the third semiconductor layer [61, 62] is interposed between the second semiconductor layer [52] and a bottom of the fourth semiconductor layer [81] and is in direct contact with said second semiconductor layer [52]; a fifth semiconductor layer [131] of the second conductivity type selectively provided in a surface of the fourth semiconductor layer [81] and opposing the third semiconductor layer [61, 62] through the fourth semiconductor layer [81]; a first main electrode [160] disposed across and connected with surfaces of the fourth and fifth semiconductor layers [81, 131]; a second main electrode [170] provided on the second main surface of the first semiconductor layer [50]; an insulating film [111, 112] provided on portions of the fourth semiconductor layer [81] interposed between the third and fifth semiconductor layers [61, 62, 131]; a control electrode [114, 115] facing the portions through the insulating film [111, 112] so that the portions form channel regions as only channel regions of the insulated gate semiconductor device.

Since Kinzer discloses his device has a hexagonal cell topology (col. 9, lines 44-59), the n-type region [60-62] forms a one continuous region (col. 11, lines 49-51).

Therefore, the insulating film [110, 111, 112] is a continuous insulating film and the gate electrode [113, 114, 115] is a continuous gate electrode.

In regards to claim 24, Kinzer further discloses a sixth semiconductor layer [51] of the second conductivity type higher in an impurity concentration (n+) than the second semiconductor layer [52] provided between the first and second semiconductor layers [50, 52].

In regards to claim 26, Kinzer further discloses the first main electrode [160] is not contacting any other semiconductor than the fourth and fifth semiconductor layers [81, 131].

In regards to claim 40, Kinzer shows all the elements of the claimed invention in fig. 20. It is an insulated gate semiconductor device, comprises: a first semiconductor layer ([50] of fig. 19) of a first conductivity type (p) having first and second main surfaces on opposite sides thereof; a second semiconductor layer ([52] of fig. ~~19~~ 20) of a second conductivity type (n) provided on the first main surface of the first semiconductor layer; a third semiconductor layer [180] of the second conductivity type higher in an impurity concentration (n+) and thinner than the second semiconductor layer [52], and provided on a surface of the second semiconductor layer [52]; a fourth semiconductor layer [81] of the first conductivity type provided on a surface of the third semiconductor layer [61, 62], wherein the third semiconductor layer [180] is interposed between the second semiconductor layer [52] and a bottom of the fourth semiconductor layer [81], and said third semiconductor layer [180] is in direct contact with said second semiconductor layer [52] and so that fourth semiconductor layer [81] does not contact with second

semiconductor layer [52]; a fifth semiconductor layer [131] of the second conductivity type selectively provided in a surface of the fourth semiconductor layer [81] and opposing the third semiconductor layer [180] through the fourth semiconductor layer [81]; a first main electrode [160] disposed across and connected with surfaces of the fourth and fifth semiconductor layers [81, 131]; a second main electrode [170] provided on the second main surface of the first semiconductor layer [50]; an insulating film [111, 112] provided on portions of the fourth semiconductor layer [81] interposed between the third and fifth semiconductor layers [180, 131]; a control electrode [114, 115] facing the portions through the insulating film [111, 112] so that the portions form channel regions as only channel regions of the insulated gate semiconductor device.

Since Kinzer discloses his device has a hexagonal cell topology (col. 9, lines 44-59), the insulating film [110, 111, 112] is a continuous insulating film and the gate electrode [113, 114, 115] is a continuous gate electrode.

In regards to claim 42, Kinzer further discloses a sixth semiconductor layer ([51] of fig. 19) of the second conductivity type higher in an impurity concentration (n+) than the second semiconductor layer [52] provided between the first and second semiconductor layers ([50, 52] of fig. 19).

In regards to claim 44, Kinzer further discloses the first main electrode [160] is not contacting any other semiconductor than the fourth and fifth semiconductor layers [81, 131].

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 23, 25, 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer.

In regards to claims 23 and 41, Kinzer differs from the claimed invention by not showing the second semiconductor layer extends through the first semiconductor layer and is partially exposed in the second main surface of the first semiconductor layer. It would have been obvious for the second semiconductor layer extends through the first semiconductor layer and is partially exposed in the second main surface of the first semiconductor layer because it depends to the switching speed of the device.

In regards to claims 25 and 43, Kinzer differs from the claimed invention by not showing the sixth semiconductor layer extends through the first semiconductor layer and is partially exposed in the second main surface of the first semiconductor layer. It would have been obvious for the sixth semiconductor layer extends through the first semiconductor layer and is partially exposed in the second main surface of the first semiconductor layer because it depends to the switching speed of the device.

6. Applicant's arguments filed 2/5/03 have been fully considered but they are not persuasive.

It is urged, in page 6 of the remarks, that Kinzer never discloses an insulating film provided on portions of the fourth semiconductor layer interposed between the third and fifth semiconductor layers and a control electrode facing the portions through the insulating film so that the portions form channel regions as only channel regions of the

insulated gate semiconductor device. Since Kinzer discloses a device having a hexagonal cell topology, the insulating film [111, 112] provided on portions of the fourth semiconductor layer [81] interposed between the third and fifth semiconductor layers [61, 62, 131] and a control electrode [114, 115] facing the portions through the insulating film [111, 112] so that the portions form channel regions as only channel regions of the insulated gate semiconductor device. Therefore, Kinzer does show all the elements of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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April 20, 2003

Steven Loke
Primary Examiner
Steven Loke